Quality Measures

Chapter 3

Source: Gajski, Dutt, Wu, Lin

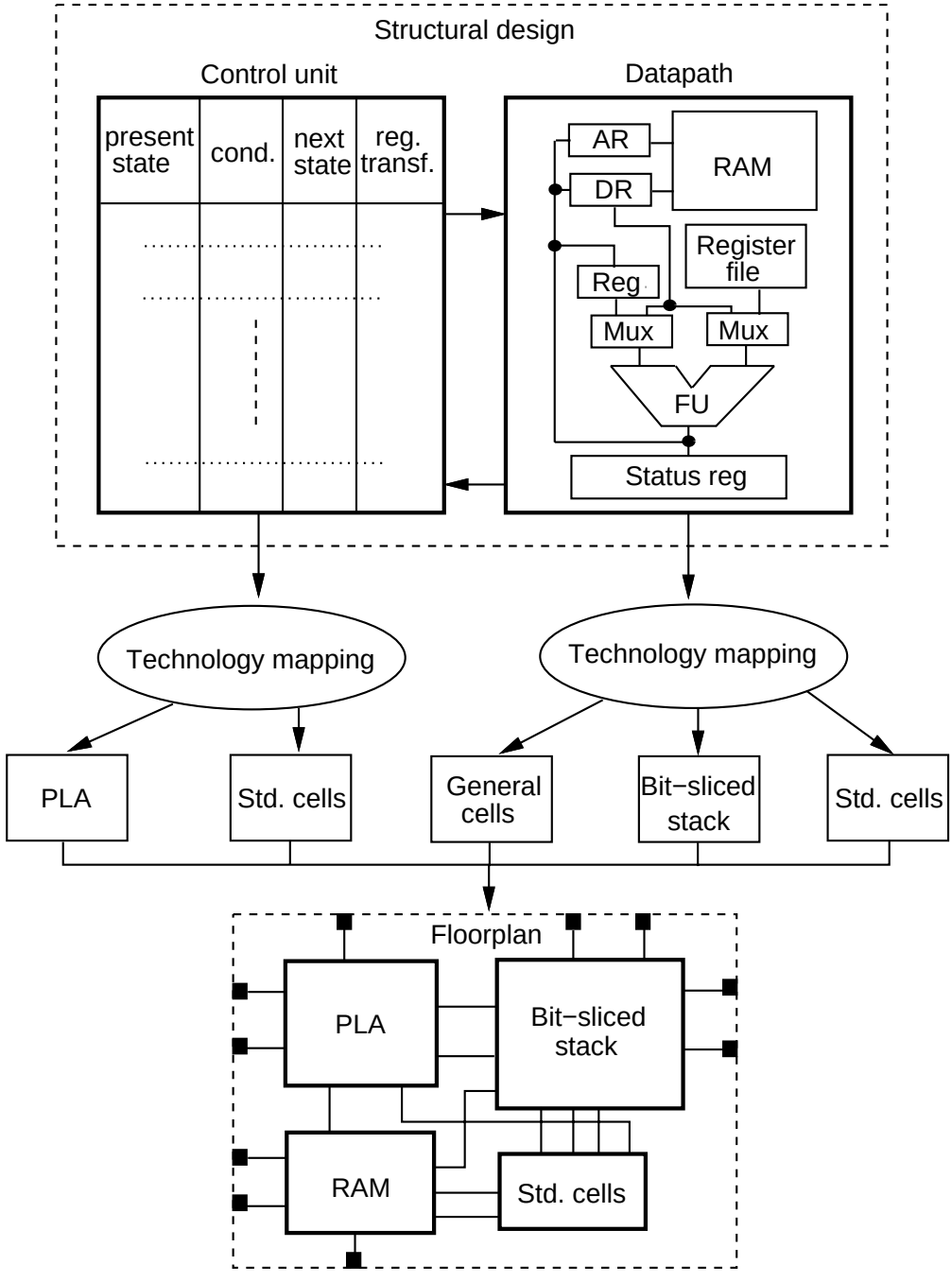
"High−Level Synthesis"

Kluwer Academic Publishers, 1992

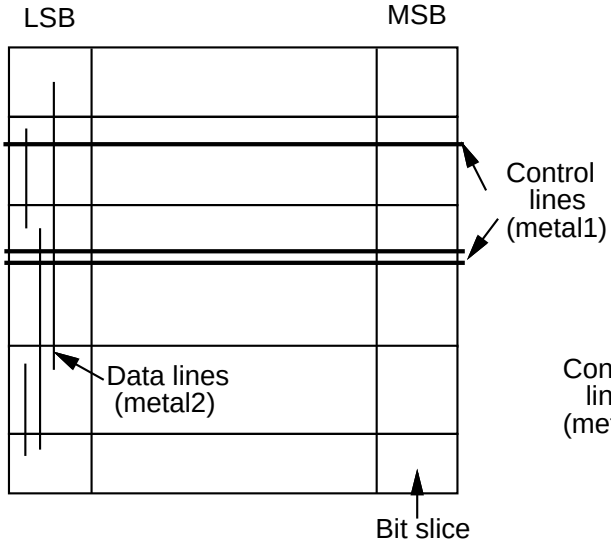
QUALITY MEASURES

1. Cost
2. Area
3. Performance
4. Power
5. Testability
6. Verifiability
7. Reliability
8. Manufacturability

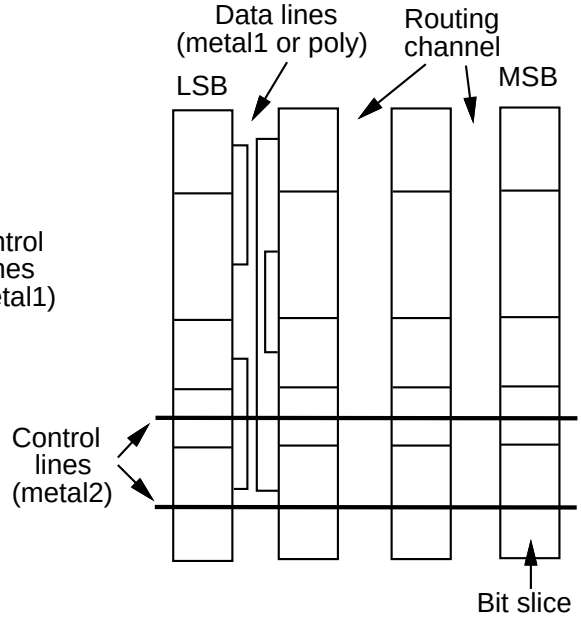
RELATIONSHIP BETWEEN STRUCTURAL AND PHYSICAL DESIGNS



DATAPATH LAYOUT ARCHITECTURE

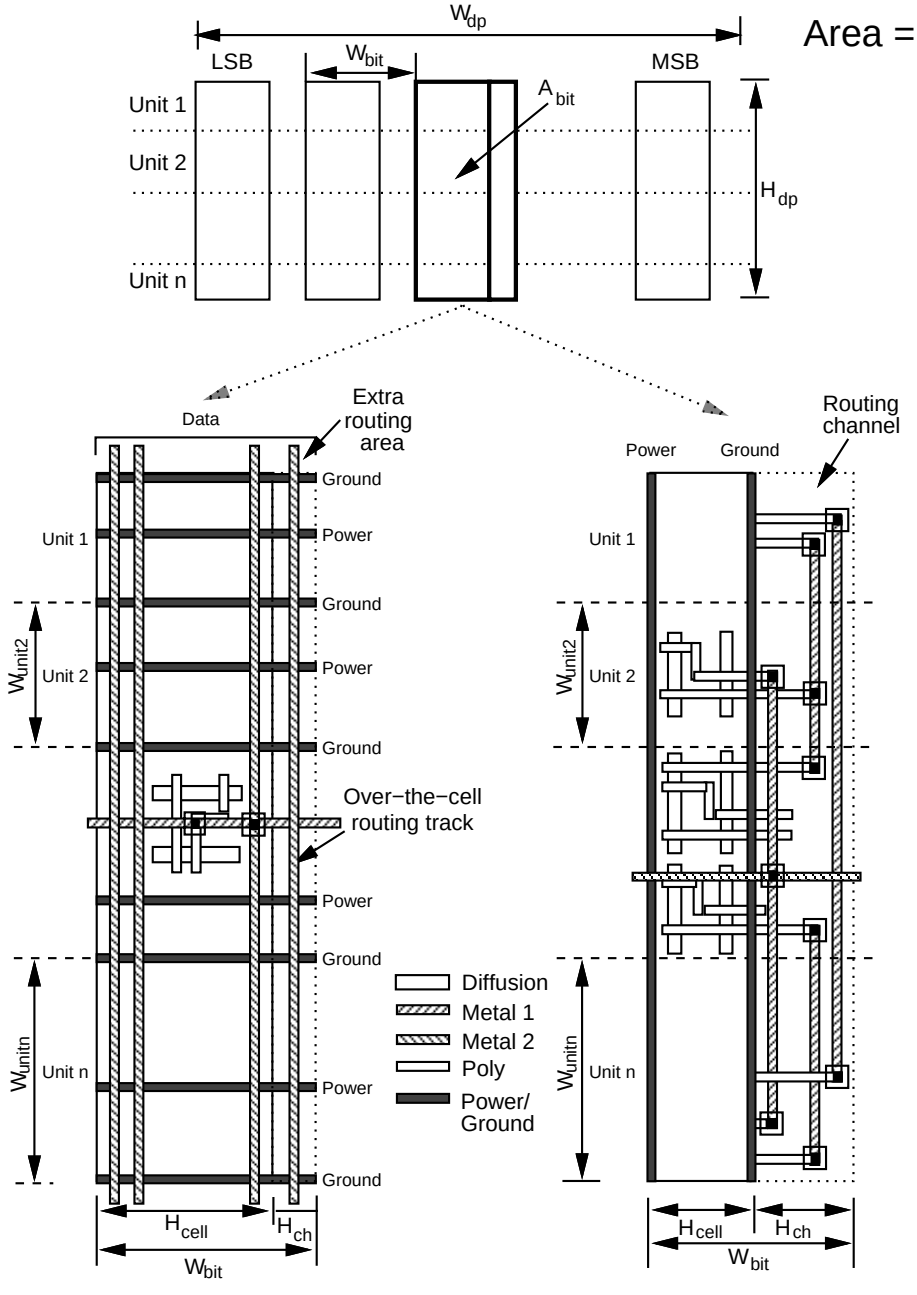


Custom Cells



Standard Cells

DATAPATH LAYOUT



Area = W_{dp} X H_{dp}

W_{unit} = $const_1$ X tr (unit)

H_{ch} = $const_2$ X # tracks $_{est}$

CONTROL UNIT LAYOUT

	Input					Output			
	I_1	I_2	I_3	I_4	I_5	O_1	O_2	O_3	O_4
	Present state		Conditions/ status			Next state		Control signals	
	p_1	p_0	s_2	s_1	s_0	r_1	r_0	c_1	c_0
State 1	0	1	1	0	0	1	0	0	1
State2	1	0	1	0	1	1	0	1	0
State3	1	0	0	0	1	1	1	1	1

State table

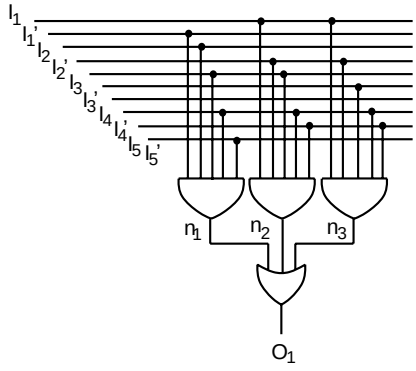
$O_1 = (I_1' I_2 I_3 I_4' I_5') \text{ OR } (I_1 I_2' I_3 I_4' I_5) \text{ OR } (I_1 I_2' I_3' I_4' I_5)$

$O_2 = (I_1 I_2' I_3' I_4' I_5)$

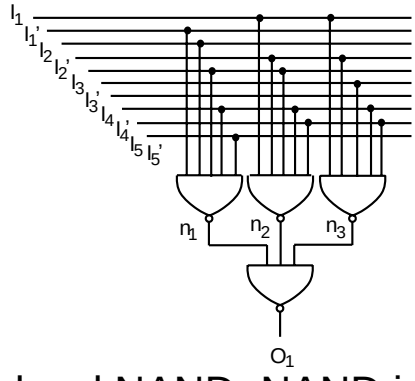
$O_3 = (I_1 I_2' I_3 I_4' I_5) \text{ OR } (I_1 I_2' I_3' I_4' I_5)$

$O_4 = (I_1' I_2 I_3 I_4' I_5') \text{ OR } (I_1 I_2' I_3' I_4' I_5)$

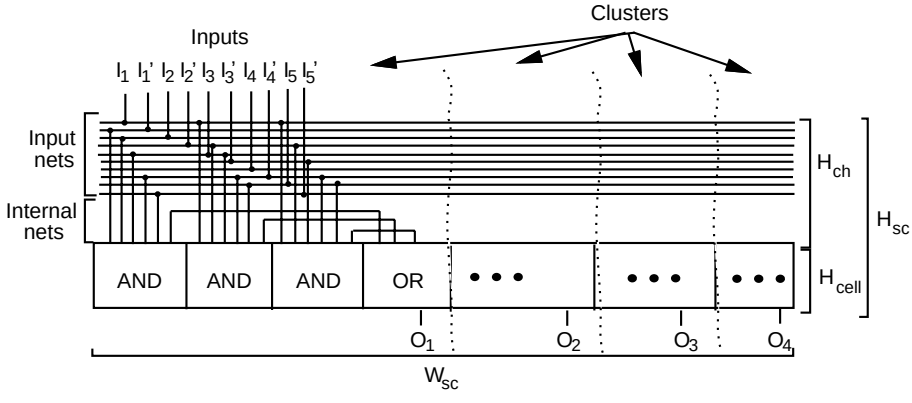
Output signals:
Boolean Equations



2−level AND−OR impl.



2−level NAND−NAND impl.

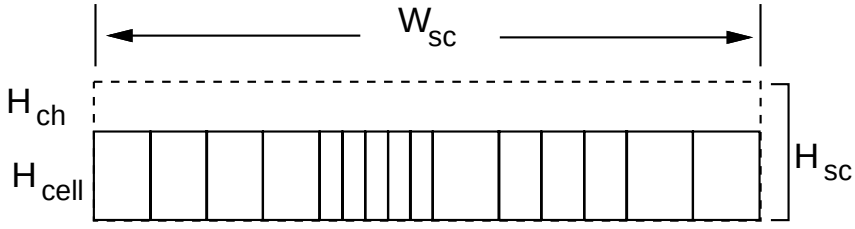


Standard cell layout

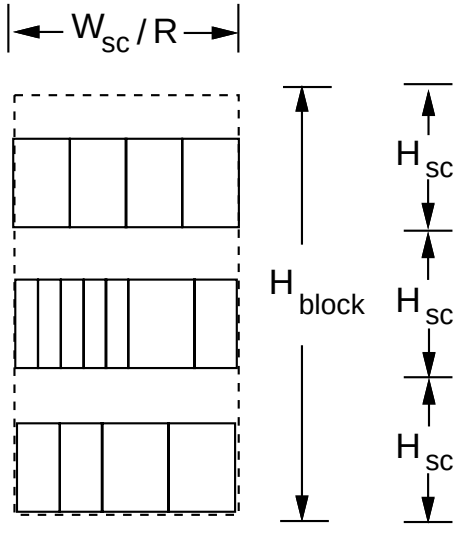
Assumptions:

1. single row
2. signal clustering
3. no sharing between signals
4. track per signal
5. no logic optimization

MULTIPLE−ROW CONTROL LAYOUT

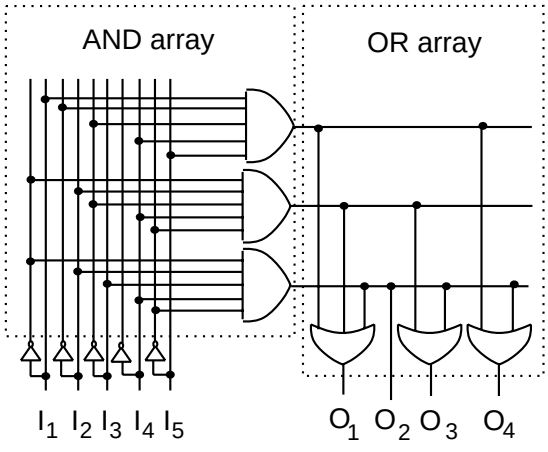


single−row implementation

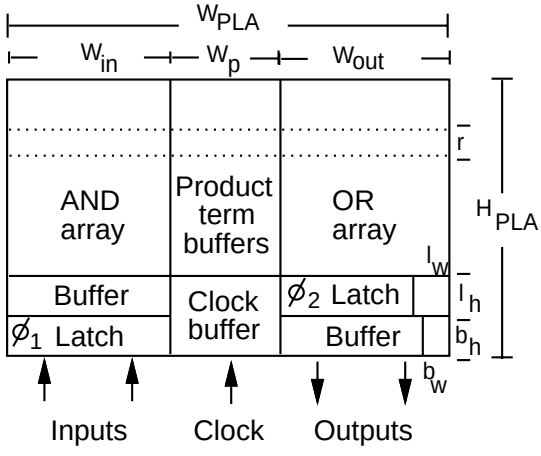


3−row implementation

PLA LAYOUT ARCHTECTURE



Logic mapping

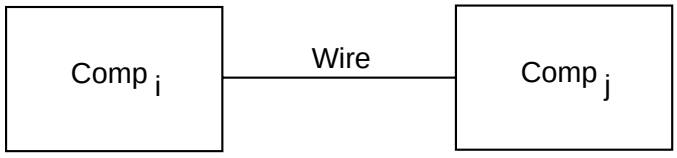


Layout model

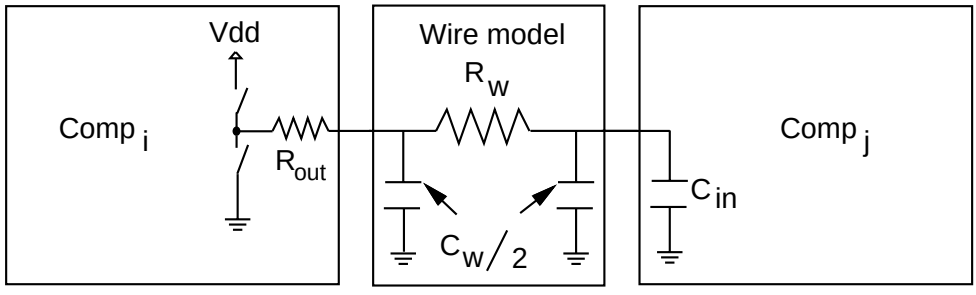
MODELING PHYSICAL DESIGN

1. Probabilistic distribution for pins, wire length
2. Placement, routing models
3. Linear algorithms (min−cut)
4. State encoding model
5. Logic minimization
6. Technology mapping
7. Transistor sizing

WIRE MODELING



RT model



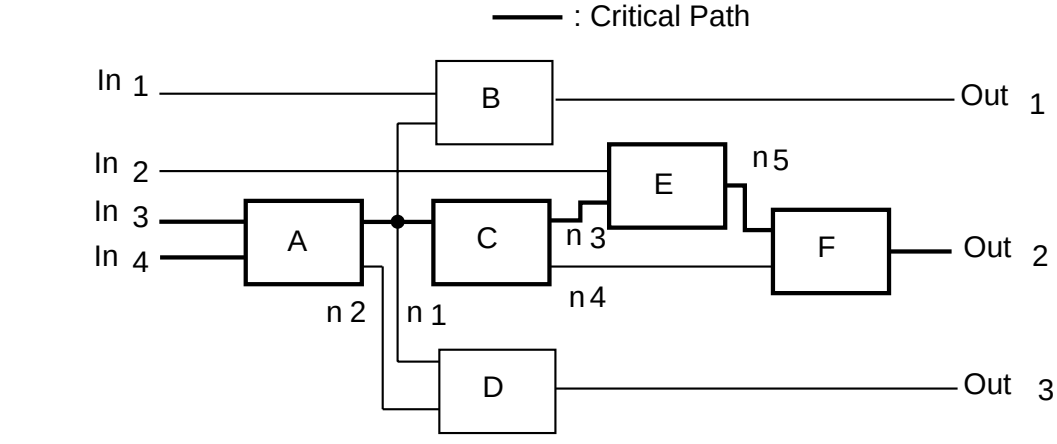
Equivalent RC delay model

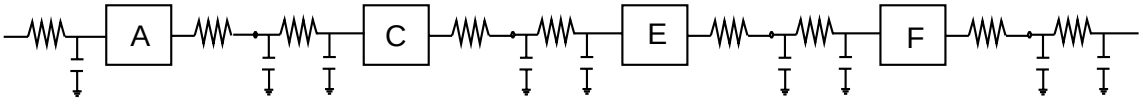
$$R_w = R_s \left(\frac{L_w}{W_w} \right)$$

$$C_w = (L_w W_w) \left(\frac{E}{t} \right)$$

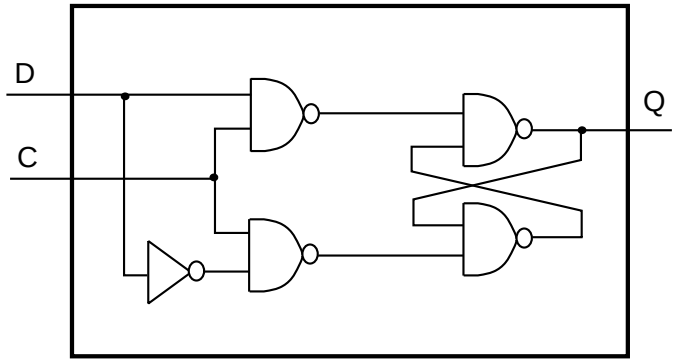
$$t_p = (R_{out} + R_w)(C_w + C_{in})$$

COMBINATORIAL DELAY

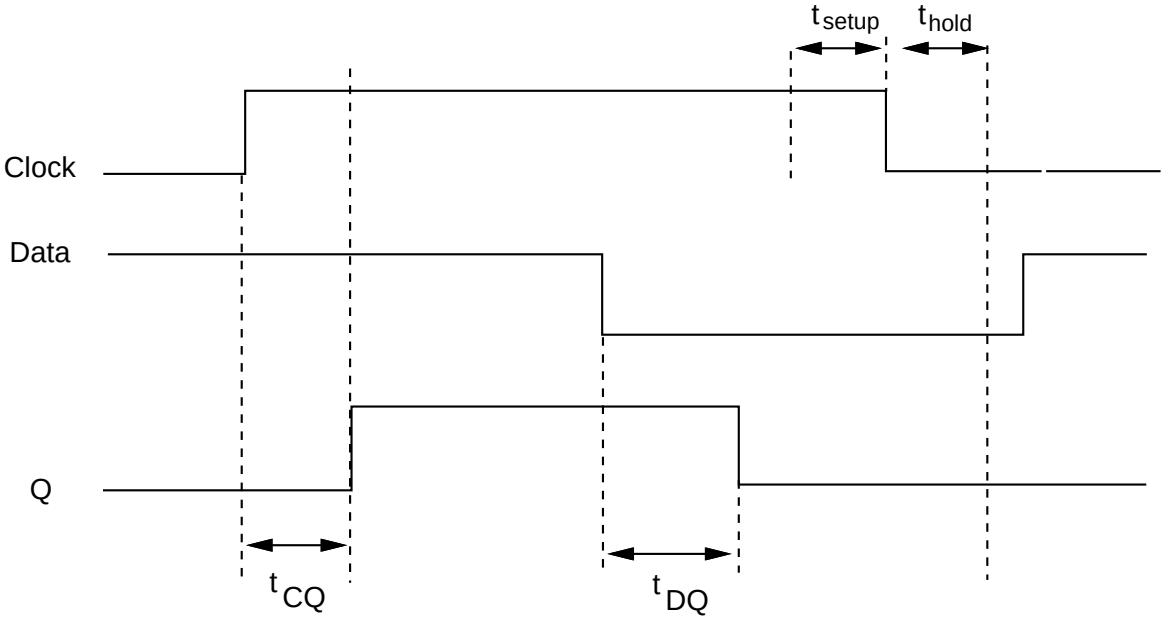




D–LATCH DELAYS

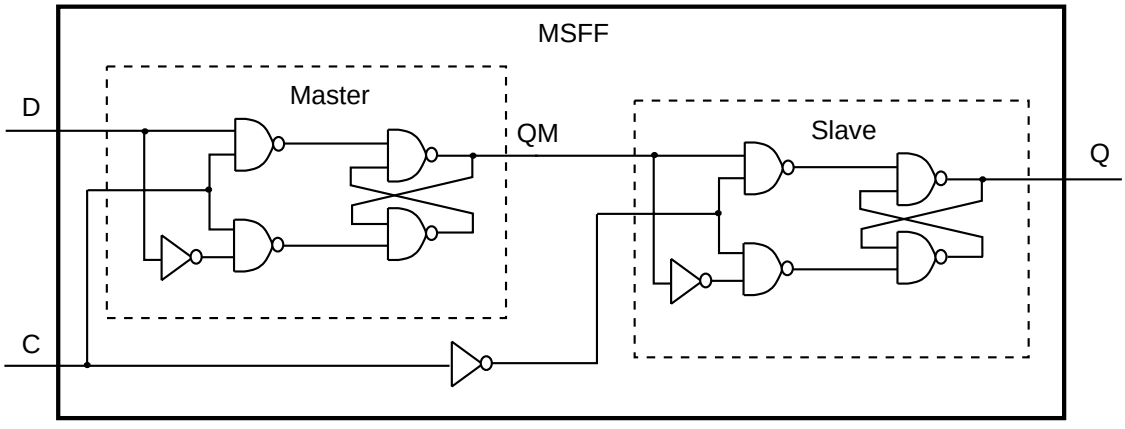


D – Latch

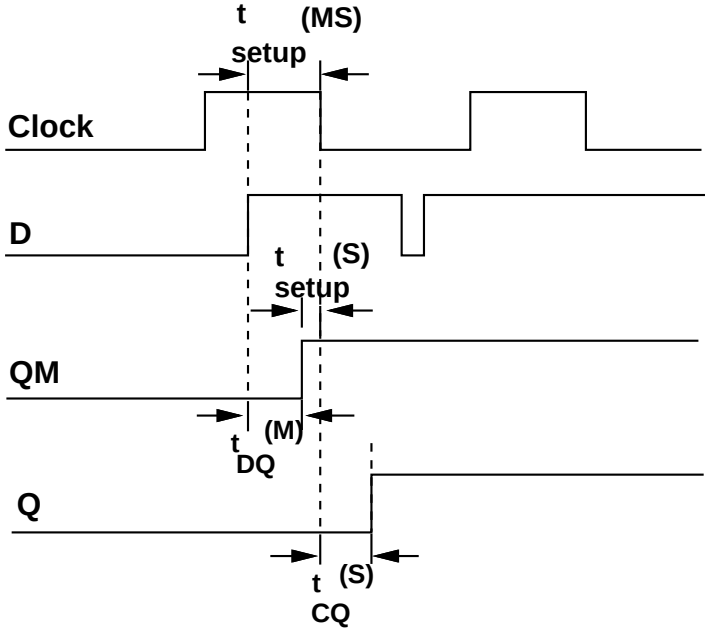


Timing Diagram

MASTER−SLAVE DELAYS

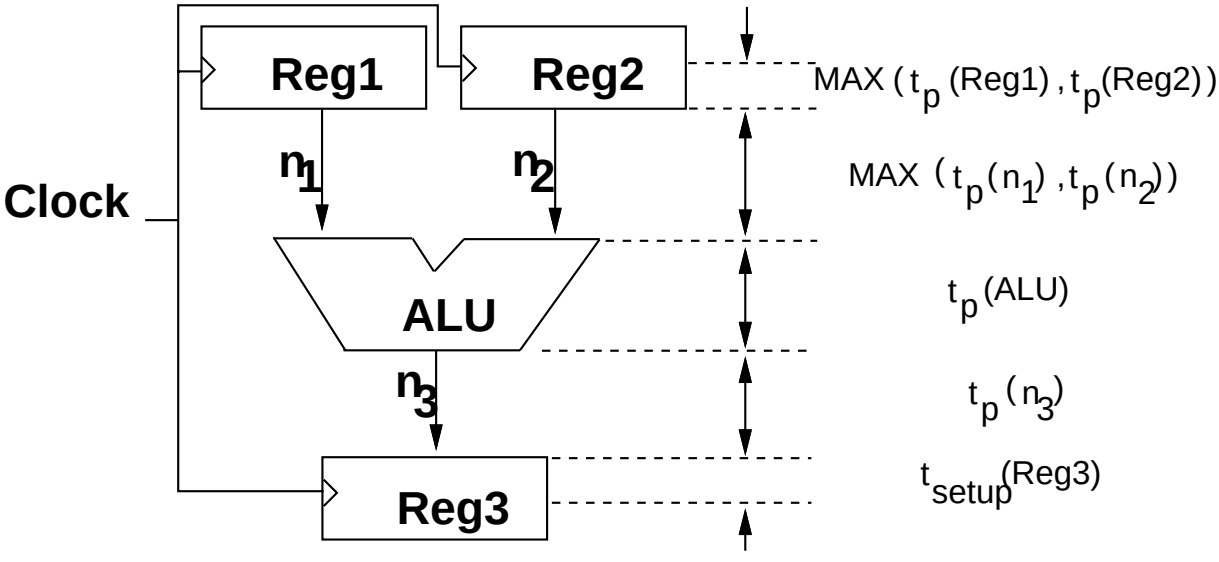


MS flip−flop

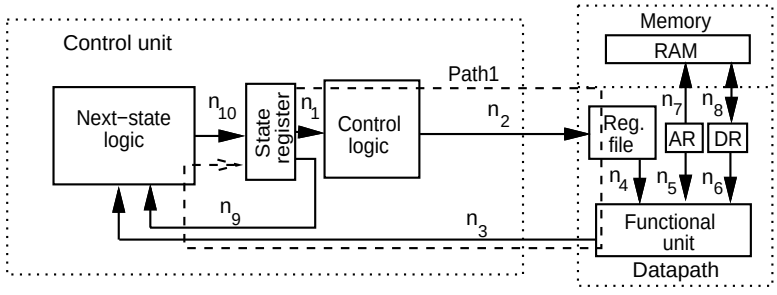


Timing diagram

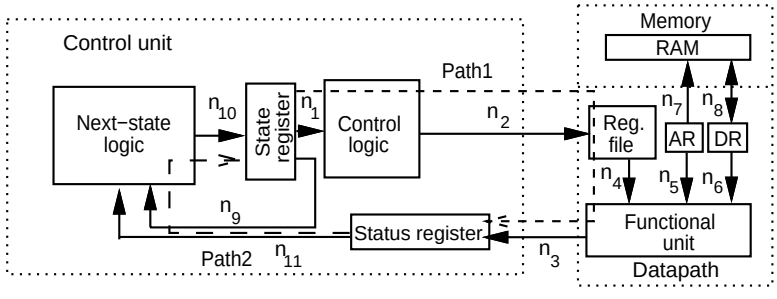
REGISTER−TRANSFER PATH



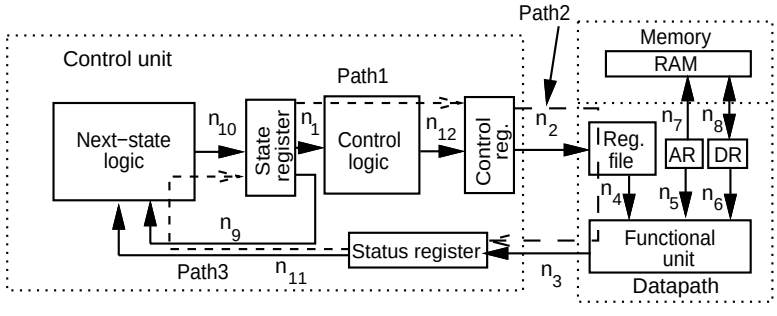
SYSTEM CLOCKING MODELS



Non−pipelined control



One−stage pipeline



Two−stage pipeliine

FUTURE DIRECTIONS

Better models

Modeling algorithms

Control Optimization

State encoding
Logic optimization

Microarchitecture optimization

Floorplanning models

Other measures

Other technologies